CLAIMS

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- 1. A memory device comprising:
- a first bank of data storage cells;
- a second bank of data storage cells; and
- a state machine configured to initiate a read operation from the second bank while currently controlling an embedded write operation to the first bank.
- 2. The memory device of claim 1 wherein the state machine comprises:
 - a front end to decode received user commands; and
 - a back end to control embedded operations including the embedded write operation in response to the user commands.
- 3. The memory device of claim 2 wherein the front end is configured to decode a burst read command while the back end controls the embedded write operation.
 - 4. The memory device of claim 2 wherein the front end is configured to permit execution of only predetermined user commands during the embedded write operation.
 - 5. The memory device of claim 4 wherein the predetermined commands include a burst read command.
 - The memory device of claim 1 further comprising:
 a valid address input to receive an indication of a user specified burst read address; and
 - a clock input for receiving a burst read clocking signal.

7:	The memory device of claim 1 further comprising:
decoding circuitry to decode a received read command; and	
one or more registers to store received write command data related to the	
	embedded write operation during execution of the embedded write
	operation.

The memory device of claim 7 further comprising:

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a clocking circuit coupled with the one or more registers to generate a command clock signal for latching command data in the one or more registers; and a masking circuit to generate a mask signal to disable the command clock signal when received command does not correspond to a valid command.

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9. The memory device of claim 1 wherein the state machine further comprises:

verification circuitry to identify a correct command sequence before initiating the embedded write operation to the first bank.

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10. A method for operating a memory comprising: receiving a command defining an embedded operation; in response to the command, initiating the embedded operation; receiving a subsequent command;

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if the subsequent command is one of an excepted predetermined subset of commands, initiating execution of the command; and otherwise, ignoring the subsequent command.

- 11. The method of claim 10 further comprising: receiving a command sequence including the command.
- 12. The method of claim 11 further comprising:

verifying commands of the command sequence.

13. The method of claim 12 further comprising:

if commands of the command sequence do not match a predetermined command sequence, terminating the embedded operation.

14. The method of claim 10 further comprising:

if the subsequent command comprises a burst read command, initiating a burst read while simultaneously executing the embedded operation.

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15. The method of claim 14 wherein the embedded operation comprises a sector erase of a sector of the memory.

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16. A method for operating a flash memory, the method comprising: in response to a received operation command, initiating an embedded operation of the flash memory; and

subsequently, during execution of the embedded operation, in response to a received read command, initiating a burst read operation of the flash memory.

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17. The method of claim 16 further comprising: receiving a sequence of commands including the operation command; if the sequence of commands does not match a predetermined sequence, suspending initiation of the embedded operation.

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18. The method of claim 16 further comprising:
during execution of the embedded operation, receiving a command;
decoding the command;

if the command corresponds to one of an excepted predetermined subset of commands, initiating the burst read operation; and otherwise, ignoring the command.

19. The method of claim 18 further comprising: storing data corresponding to the received operation command; and after storing, decoding subsequent commands including the command.

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